WHAT IS CLAIMED IS:

1. A differential amplifier circuit comprising:

a first differential amplifier circuit including a differential input portion comprising a pair of MOS transistors of a first conductivity type; and

a second differential amplifier circuit including a differential input portion comprising a pair of MOS transistors of a second conductivity type, wherein

a first signal and a second signal having a cycle corresponding with that of the first signal are input to both of said first and second differential amplifier circuits to generate differential amplification outputs based on said first and second signals and wherein the differential amplification outputs of said first and second differential amplification circuits are combined to provide an output.

2. A differential amplifier circuit comprising:

a first MOS transistor of a first conductivity type having a source, a drain and a gate, and receiving a first signal at the gate thereof;

a second MOS transistor of the first conductivity type having a source, a drain and a gate, and receiving a second signal having a cycle corresponding with that of said first signal at the gate thereof;

a first current mirror circuit comprising a third and a fourth MOS transistors of a second conductivity type each

having a source, a drain and a gate, the drains of said third and fourth MOS transistor being connected to the drains of said first and second MOS transistors, respectively, the gates of the third and fourth MOS transistors connected to each other and the gate and drain of said third MOS transistor;

a fifth MOS transistor of the second conductivity type having a source, a drain and a gate, and receives the first signal at the gate thereof;

a sixth MOS transistor of the second conductivity type having a source, a drain and a gate, and receiving the second signal at the gate thereof;

a second current mirror circuit comprising a seventh and an eighth MOS transistors of the first conductivity type each having a source, a drain and a gate, the drains of said seventh and eighth MOS transistors being connected to the drains of said fifth and sixth MOS transistors, respectively, the gates of the seventh and eighth MOS transistors being connected each other and the gate and drain of said seventh MOS transistor being connected; and

an output buffer circuit for generating an output signal based on a signal generated at the drain of said fourth MOS transistor and a signal generated at the drain of said eighth MOS transistor.

3. The differential amplifier circuit according to claim 2, wherein the gates of said third and fourth MOS transistors and

the gates of said seventh and eighth MOS transistors are connected, and said output buffer circuit is a CMOS inverter having an input terminal being connected to the connection point between the drain of said fourth MOS transistor and the drain of said eighth MOS transistor.

4. The differential amplifier circuit according to ~~claim~~ Claim 3 ~~2~~, wherein said output buffer circuit comprises a ninth MOS transistor of the second conductivity type having a source, a drain and a gate which is connected to the drain of said fourth MOS transistor and a tenth MOS transistor of the first conductivity type having a source, a drain and a gate which is connected to the drain of said eighth MOS transistor, and the drains of said ninth and tenth MOS transistors are connected to each other to generate an output signal at the connection point.

5. The differential amplifier circuit according to claim 4, wherein the sources of said first and second MOS transistors are connected to a first potential source through a first current control circuit common to both of them, the sources of said third and fourth MOS transistors are connected to a second potential source, the sources of said fifth and sixth MOS transistors are connected to said second potential source through a second current control circuit common to both of them, the sources of said seventh and eighth MOS transistors are connected to said first potential source, and the sources of said ninth and tenth MOS transistors are connected to said

second and first potential sources, respectively.

6. A differential amplifier circuit comprising:

a first MOS transistor of a first conductivity type having a source, a drain and a gate, and receiving a first signal at the gate thereof;

a second MOS transistor of the first conductivity type having a source, a drain and a gate, and receiving a second signal having a cycle corresponding with that of said first signal at the gate thereof;

a first current mirror circuit comprising a third and a fourth MOS transistors of a second conductivity type each having a source, a drain and a gate, the drains of said third and forth MOS transistors being connected to the drains of said first and second MOS transistors, respectively, the gates of the third and fourth MOS transistors being connected to each other and the gate and drain of said third MOS transistor being connected;

a fifth MOS transistor of the second conductivity type having a source, a drain and a gate, and receiving the first signal at the gate thereof;

a sixth MOS transistor of the second conductivity type having a source, a drain and a gate, and receiving the second signal at the gate thereof;

a second current mirror circuit comprising a seventh and an eighth MOS transistors of the first conductivity type each

having a source, a drain and a gate, the drains of said seventh and eight MOS transistors being connected to the drains of said fifth and sixth MOS transistors, respectively, the gates of the seventh and eighth MOS transistors being connected each other and the gate and drain of said seventh MOS transistor being connected; and

at least one of a first and a second current control circuits, said first current control circuit being for commonly connecting the sources of said first, second, seventh and eighth MOS transistors to a first potential source and controlling a current flowing therein, and said second current control circuit commonly connecting the sources of said third, fourth, fifth and sixth MOS transistors to a second potential source and controlling a current flowing therein,

the drains of said fourth and eight MOS transistors being connected to provide a connection point as an output terminal, and the gates of said third and fourth MOS transistors being connected to the gates of said seventh and eighth MOS transistors.

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